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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DOLE, TIMOTHY J	
ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 08/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/747,734	DAVIDSON ET AL.	
	Examiner	Art Unit	
	Timothy J. Dole	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Malek-Khosravi et al.

Malek-Khosravi et al. discloses an integrated circuit comprising: means for generating a test signal (Fig. 1) having a predetermined pulse width (column 2, lines 59-66) in response to a control input (Fig. 1; and column 2, line 33); and means for predicting failure of part or all of said integrated circuit in response to said test signal (column 3, lines 17-28 and line 37). It should be noted that Malek-Khosravi et al. discloses that the test signal starts from a maximum width of w_n, which is a predetermined pulse width. Even though the pulse widths in the test sequence change, there still exists a predetermined pulse width, w_n, as is claimed. Also, Malek-Khosravi et al. does disclose the function of predicting failure of part or all of the integrated circuit in response to a test signal, as presently claimed. Malek-Khosravi et al. detects a failure when the width of the test pulses gets too small. However, the failure could result from other means, such as human error. Therefore, the detected error is only assumed, or predicted, to have been caused in response to the test signal.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10 and 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad et al. in view of Malek-Khosravi et al.

Regarding claim 1, Ahmad et al. discloses an integrated circuit comprising: a test circuit (upper half, Fig. 2; and column 3, lines 62-63) configured to generate a test signal (53 and 55, Fig. 2; and column 6, lines 14 ff) that predicts failure of said integrated circuit (column 1, lines 16-17; column 2, lines 63-67; column 4, line 29).

Ahmad et al. does not expressly disclose a test signal having a predetermined pulse width in response to a control input, wherein said test signal tracks process corners and which can be used to predict failure of said integrated circuit. Albeit, Ahmad et al. discloses (Figs. 8-10) various methods for performing a self-test on the built-in circuits.

Malek-Khosravi et al. discloses an integrated circuit chip configured to generate a test signal with a predetermined pulse width (Fig. 2; and column 1, lines 9-24) in response to a control input (Fig. 1; and column 2, lines 31-34), and to determine the minimum pulse width in order for the circuit to operate properly (column 1, lines 21-24) by tracking process corners (Fig. 2). It should be noted that as stated in claim 11 above, the test signal of Malek-Khosravi et al. has a predetermined pulse width.

At the time of the invention, it would have been obvious for a person of ordinary skill in the art to have combined into Ahmad et al. the teachings of Malek-Khosravi et al., for the purpose of obtaining an integrated-circuit test circuit that can be used to predict failure of the integrated circuit, so that circuits with a high probability of failure can be eliminated from further testing and/or can be repaired.

Regarding claim 2, Ahmad et al. discloses that the control input (53, Fig. 2) comprises a write enable input (Fig. 8; and column 9, lines 26 ff).

Regarding claim 3, Ahmad et al. discloses a transition to a write enable input (column 9, lines 39-45).

Regarding claim 4, Ahmad et al. discloses using transition from HIGH to LOW logic levels (column 3, lines 1-15).

Regarding claims 5 and 6, Ahmad et al. does not expressly disclose that the pulse width can be selected by the user with various inputs.

Malek-Khosravi et al. discloses that the pulse width can be selected by the user with various inputs (Fig. 1; and column 2, line 66 to column 3, line 4).

At the time of the invention, it would have been obvious to incorporate into Ahmad et al. the teaching of Nlalek-Khosravi et al. for the purpose of parametrically varying the pulse width as desired.

Regarding claim 7, Ahmad et al. discloses that the configuration is fuse programmable (column 10, lines 25 ff).

Regarding claim 8, Ahmad et al. discloses that the configuration inputs are determined by a metal masking step during fabrication (column 3, lines 39-51).

Regarding claim 9, Ahmad et al. discloses that the technique can be used to test static random access memory (SRAM) cells (column 7, lines 44-48).

Regarding claim 10, Ahmad et al. discloses that the test circuit is configured to predict failure of one or more cells (Figs. 3-5; column 4, lines 23-32; and column 9, line 58 to column 10, line 10).

Regarding method claim 12, Ahmad et al. discloses a method of testing an integrated circuit comprising the steps of: (A) entering a test mode (column 9, line 20); (B) measuring the operation of said integrated circuit (column 8, lines 3 ff) in response to a test signal generated (by the oscillator 55) on the integrated circuit (Fig. 2) in response to a control input 53); and (C) predicting said failure of said integrated circuit in response to failure of said operation (column 6, lines 33-41).

Ahmad et al. does not expressly disclose that the test signal has a predetermined pulse width.

Malek-Khosravi et al. discloses a method of testing an integrated circuit chip in which the test signal has a predetermined pulse width (column 3, lines 17 ff). It should be noted that as stated in claim 11 above, the test signal of Malek-Khosravi et al. has a predetermined pulse width.

Therefore, at the time of the invention, it would be obvious for a person of ordinary skill in the art to have combined into Ahmad et al. the teaching of Malek-Khosravi et al., for the purpose of a method for predicting failure of an integrated circuit, so that circuits with a high probability of failure can be eliminated from further testing and/or can be repaired.

Regarding claims 13 and 14, Ahmad et al. discloses a write operation and a write pulse (column 9, lines 46 ff).

Regarding claim 15, Ahmad et al. discloses a pulse width determined by the data setup (oscillator 55).

Regarding claim 16. Ahmad et al. discloses life testing (abstract).

Regarding claim 17, Ahmad et al. discloses a sorting step following the testing (column 10, lines 23 ff).

Regarding claim 18, Ahmad et al. discloses repairing faulty integrated circuits (column 2, line 39).

Regarding claim 19, Ahmad et al. discloses that the failure of said integrated circuit is related to a poor contact in cross-coupled latch transistors of a memory cell (column 6, lines 33-41). It should be noted that since failure of memory cells is caused by poor contacts in cross-coupled latch transistors, it follows that the errors detected by Ahmad et al. are therefore caused by the poor contacts in the cross-coupled latch transistors.

Regarding claim 20, Ahmad et al. discloses, even within the context of well known prior art, voltage control of the tests (column 3, lines 1-15).

Regarding claims 21-23, Ahmad et al. does not expressly disclose a plurality of pulse widths, a sequence of pulse widths and different circuits for generating them.

Malek-Khosravi et al. discloses a plurality of pulse widths (abstract; and Fig. 2), a sequence of pulse widths (Fig. 2; column 2, line 63; and column 3, lines 9-11) and different circuits for generating them (Figs. 1-6).

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine into Ahmad et al., the teachings of Malek-Khosravi et al., for the purpose of having versatile control over the pulse-width inputs.

New Claim

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is unclear how in claim 24 "said failure is independent of said test signal" (lines 1-2) when in claim 1 "said test signal (i) tracks process corners and (ii) predicts a failure of said integrated circuit" (lines 4-5). If the test signal is being used to predict the failure, then the failure must depend on the test signal. If no test signal were generated, no failure could be predicted. Therefore the failure must be dependent on the test signal.

Response to Arguments

7. Applicant's arguments filed April 21, 2003 have been fully considered but they are not persuasive.

8. In response to the Applicant's argument with respect to claims 1, 11 and 12, that Malek-Khosravi et al. fails to teach "the identical function of generating a test signal having a predetermined pulse width in response to a control input" (page 13, lines 4-6), and "the identical

function of predicting failure of part or all of the integrated circuit in response to a test signal" (page 13, lines 11-13) it should be noted that as shown in claim 11, above, Malek-Khosravi et al. does disclose a predetermined pulse width, w_n, and a failure prediction in response to a test signal as claimed.

Final Rejection

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J. Dole whose telephone number is 703-305-7396. The examiner can normally be reached on Mon. thru Fri. from 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on 703-308-0750. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TJD
August 7, 2003

N. Le
Supervisory Patent Examiner
Technology Center 2800